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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,496	10/16/2003	Chih-Jen Huang	025796-00010	5365

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EXAMINER

YOHA, CONNIE C

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/685,496

Applicant(s)

HUANG, CHIH-JEN

Examiner

Connie C. Yoha

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
- Paper No(s)/Mail Date _____.

CONNIE C. YOHA
PRIMARY EXAMINER



- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities:

Applicants should review and correct the entire specification for misspelling, for example: on page 3 line 21, change "ot" to --of--, and page 8, line 19, change "salient" to --silent--. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

The description of the drain region 20 stated on page 3, line 6 cannot be found in figure1 as mentioned. Correction is required.

Applicant is required to submit a proposed drawing correction in response to this Office action. However, formal correction of the noted defect(s) can be deferred until the examiner allows the application. Also note MPEP 608.02 (r) and (v).

Claim Rejections - 35 USC § 112

4. Claim 4, 7-8 and 10-11, rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 4 and 7, it is vague and not clear, therefore cannot be understood by the examiner what is meant on line 2 of claim 7 "wherein said source line is divided along a bit direction by using **an isolation structure**". Examiner cannot determine what is meant by an isolation structure.

With regard to claim 8, there is insufficient antecedent basis for the limitations of "a supply voltage". Note, in claim 5, a supply voltage is applied to the control gate, not to the N-type well region as claim 8 claimed.

With regard to claim 10, it is also vague and not clear, therefore cannot be understood by the examiner what is meant on line 6-7 of claim 10 "applying an erase voltage to said P-type drain region to cause tunneling of electrons from a floating to said N-type well region and to said N-type well region". Does the applicant meant to say, ... causing tunneling of electrons to float from said N-type well region **to said Drain region?**

With regard to claim 11 is rejected due to the rejections of the parent claim 10.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2, 5, 9 and 11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With regard to claims 2, 5 and 11, the limitation of “wherein said erase voltage **between about 12 volts**” is not described in the specification.

With regard to claim 9, the limitation of “wherein said cell is programmed by applying a **negative supply voltage between 6-10** to said P-type drain region” on line 1-3 is not described in the specification. In fact, page 12, line 4 of the specification specifically disclosed that “memory cell is programmed by applying a **negative voltage around -4 to -6 volts** to the drain region to induce hot electron”.

Also with regard to claim 9, the limitation of “a negative threshold voltage is of **about 2 Volts** applied to said word line” is not described in the specification. In fact, page 12, line 21-23 specifically discloses “the gate voltage Vg is ...around **-4 volts**.”

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Onakado et al, Pat. No. 5818761.

With regard to claim 1, Onakado discloses a non-volatile memory cell structure, said structure comprising: an N-type well region (fig. 51, 1) in a substrate, a channel region (fig. 51, 8) between a P-type source region (fig. 51, 2/3) and a P-type drain region (fig. 51, 3/2), wherein the conductivity type of said P-type is opposite to said N-type; a first insulator layer (fig. 51, 4) on the surface of said N-type well region (fig. 51, 1); a floating gate (fig. 51, 5) overlying said first insulator layer (fig. 51, 4); a second insulator layer (fig. 51, 6) on said floating gate (fig. 51, 5); and a control gate (fig. 51, 7) on said second insulator layer (fig. 51, 6), wherein said non-volatile memory cell is erased by applying an erase voltage (fig. 51, 5-12V) to said P-type drain region (fig. 51, 3/2, drain and source region are inherently known in the semiconductor art to be interchangeable), applying a supply voltage (fig. 51, -5 to -12V), and said erase voltage (fig. 51, 5-12V) applied to the N-type well region (fig. 51, 1).

With regard to claim 2, as far as understood, Onakado discloses wherein said erase voltage between about 12 volts (fig. 51, 5-12V).

With regard to claim 3, Onakado discloses a source line (fig. 11, SL) couple to said P-type source region (also with regard to claim 6), said source line exhibits floating (fig. 51, element 3/2, note, drain and source are inherently known in the semiconductor art to be interchangeable) (col. 5, line 11-16).

With regard to claim 4, as far as understood, Onakado discloses wherein said source line is divided by an isolation structure along a bit line direction (fig. 11, SL runs parallel is along a bit line SB11-SB01 and MB1-MB0 direction) (also with regard to claim 7).

With regard to claim 5, as far as understood, Onakado discloses a non-volatile memory cell structure, said structure comprising: an N-type well region (fig. 51, 1) in a substrate, a channel region (fig. 51, 8) between a P-type source region (fig. 51, 2/3) and a P-type drain region (fig. 51, 3/2), wherein the conductivity type of said P-type is opposite to said N-type; an insulator layer (fig. 51, 4) overlying said N-type well region (fig. 51, 1); a gate transistor (fig. 51, 7) on said insulator layer; said gate transistor comprise a control gate (fig. 51, 7) coupled to a word line (fig. 11, WL), said P-type drain region (fig. 49A, 3/2) coupled to a bit line (fig. 11, example SB11-SB11); wherein said cell is erased by applying an erase voltage between about 12 volts (fig. 51, 5-12V) to said P-type drain region (fig. 51, element 3/2, drain and source are inherently known in the semiconductor art to be interchangeable), and applying a supply voltage (fig. 51, -5 to -12V) to the control gate (fig. 51, 7).

With regard to claim 8, Onakado discloses wherein a supply voltage applied to said N-type well region (fig. 51, 1) is erase voltage (fig. 51, 5-12V).

With regard to claim 9, as far as understood, Onakado discloses wherein said cell is programmed by applying a negative supply voltage between 6-10 (fig. 49A, -3 to -10V) to said P-type drain region (fig. 49A, 3) to induce hot electrons, and a negative threshold voltage is of about 2 Volts applied to said wordline (fig. 52).

With regard to claim 10, as far as understood, Onakado discloses a method for erasing non-volatile memory cell having a P-type substrate (fig. 10, 20) and an N-type well region (fig. 10, 24) therein, a channel region (fig. 51, 8) between a P-type drain region (fig. 51, 3/2) and a P-type source region (fig. 51, 2/3), said method comprising the steps of: applying an erase voltage (fig. 51, 5-12V) to said P-type drain region (fig. 51, 2/3) to cause tunneling of electrons from a floating gate to said N-type well region and to said N-type well region, wherein said P-type drain region (fig. 51, 2/3) coupled to a bit line (fig. 11, SBL and MBL); applying a supply voltage (fig. 51, -5 to -12V) to a control gate (fig. 51, 7), wherein said control gate (fig. 51, 7) coupled to a word line (fig. 11, WL); and grounding said word line of unselected cell and said bit line of unselected cell to cause the P-type drain region as an inhibit switch (col. 21, line 43-45).

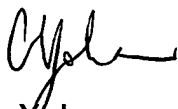
With regard to claim 11, as far as understood, Onakado discloses wherein said erase voltage is of about 12 volts (fig. 51, 5-12V).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Amin et al (5455793), Kato et al (5793678) and Han et al (6731544) disclose a memory device having program and erase operation.
9. When responding to the office action, Applicants= are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.
10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.
12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov> should you

Art Unit: 2827

have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



C. Yoha

March 2005



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